REMARKS

Claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 remain pending in the application.

Claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 over Tal in view of Lucent Technologies and Lange

In the Office Action, claims 1-3, 6-8, 10-12, 15-17, 19-21 and 24-26 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over U.S. Patent No. 6,662,254 to Tal et al. ("Tal") in view of *Lucent Technologies delivers new field-programmable system chips for high speed PCI bus and backplane data interfaces* ("Lucent Technologies"), with claims 5, 14 and 23 rejected under 35 U.S.C. §103(a) as allegedly being obvious over Tal in view of U.S. Patent No. 6,457,091 to Lange et al. ("Lange"). The Applicants respectfully traverse the rejection.

Claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 recite a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application.

The Examiner acknowledges that Tal fails to disclose "that the serial channel comprising 4 full duplex pair can be 'scalable' depending on a bandwidth needed for a particular application (See Examiner's Answer, page 6). However, the Examiner alleged that "Lucent Technologies discloses the use of the ORT4622 half bridge (page 1, 4th paragraph) including field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and containing 'a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used), see page 1, 4th paragraph, for providing design flexibility, functionality, and performance." (See Examiner's Answer, page 6 and 7). The Examiner alleged that the "ORT4622 half bridge is clearly "scalable" depending on the bandwidth needed and the fact that the ORT4622 half bridge contains a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used clearly indicates that less then 4 channels can be sued when less bandwidth is needed" (See Examiner's Answer, page 7).

Lucent Technologies appears to disclose the ORT4622 that has four channels each being 622 megabit-per-second, 2.5 gbps when all 4 channels are used (See page 1). Thus, although Lucent Technologies discloses the scalability of the ORT4622 chip, Lucent Technologies fails to disclose or suggest connection of **TWO** ORT4622s, much less disclose or suggest a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26.

Moreover, the Examiner alleges that "the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that the Applicants employ." (Examiner's Answer, page 7). The reason Lucent Technologies' ORT4622 is the same ORT4622 that Applicants employ is that the Examiner simply found a reference that **reiterates** what Applicants disclose in their specification. The Applicants are unsure of what purpose finding a prior art reference to reiterate what Applicants disclose in their specification served. Lucent Technologies STILL fails to disclose or suggest connection of **TWO** half bridge circuits for any reason, much less disclose or suggest a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26.

Moreover, "Teachings of references can be combined only if there is some suggestion or incentive to do so." In re Fine, 5 USPQ2d 1596,1600 (Fed. Cir. 1988) (quoting ACS Hosp. Sys. v. Montefiore Hosp., 221 USPQ 929, 933 (Fed. Cir. 1984)) (emphasis in original). Nothing within Tal nor Lucent Technologies suggests modifying Tal to replace Tal's disclosed PCI serialized with **TWO** ORT4622s. Thus, any modification of Tal without some suggested need to simply arrive at the claimed features is based on improper hindsight.

Moreover, the Examiner alleged that the motivation to modify Tal to replace the half bridge on each side of the PCI bus segments of Tal is to provide

flexibility/scalability, functionality, and speed/performance as disclosed by Lucent Technologies (See Examiner's Answer, page 7). However, the Examiner's motivation to modify Tal is simply Lucent Technologies disclosed benefits associated with the ORT4622 chip. The Examiner has still failed to provide motivation why one of ordinary skill in the art would be motivated to **modify Tal** that fails to disclose any deficiencies that would suggest such a modification.

Moreover, the Examiner alleged that Applicants argued in the Appeal Brief filed December 21, 2005 at pages 5 and 6 that the ORT4622 is not "scaleable" (See Examiner's Answer, page 15). However, a reading of the Appeal Brief filed December 21, 2005 reveals that Applicants never argued that an ORT4622 is not scaleable. In fact, as the Examiner points our Applicants' disclosure discloses use of two ORT4622s to provide scalability (See Applicants' disclosure, Fig. 1). Applicants argued in the Appeal Brief filed December 21, 2005 that the Examiner had failed to provide support for the allegation that CompactPCI and FPGAs are scaleable.

Lang is relied on to allegedly make up for the deficiencies in Tal to arrive at the claimed features of claims 5, 14 and 23. In particular, Lange is relied on to disclose PCI buses operating at difference frequencies (See Examiner's Answer, page 9). However, as discussed below the Examiner acknowledges that Lange fails to disclose "scaleable" signal lines (See Examiner's Answer, page 11). Thus, Tal which the Examiner acknowledges fails to disclose "scaleable" signal lines in view of Lange which the Examiner acknowledges fails to disclose "scaleable" signal lines would STILL fail to disclose or suggest "scaleable" signal lines, i.e., a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 5, 14 and 23.

The Examiner alleges that the **only** issue at question is whether the serial channel comprising a plurality of data paths, as disclosed by the prior art is "scalable depending on a bandwidth needed for a particular application (See Examiner's Answer, page 15). However, Applicants are NOT claiming to have

invented scalable data paths, but application of scalable data paths between **TWO** half bridge circuits, which the cited prior art fails to disclose or **SUGGEST**. Thus, the issue is whether it is obvious to modify the Examiner's prior art to arrive at the claimed features. As discussed above and below, there is NO motivation to modify the Examiner's primary references that the Examiner acknowledges lack any type of scalability, and which lack any disclosed need for scalability.

Accordingly, for at least all the above reasons, claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 over Lange in view of Lucent Technologies and Official Notice

In the Office Action, claims 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25 and 26 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over U.S. Patent No. 6,457,091 to Lange et al. ("Lange") in view of Lucent Technologies, with claims 6, 15 and 24 rejected under 35 U.S.C. §103(a) as allegedly being obvious Lange in view of Official Notice. The Applicants respectfully traverse the rejection.

Claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 recite a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application.

The Examiner acknowledges that Lange fails to disclose a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application (See Examiner's Answer, pages 9). However, as discussed above the Examiner alleged that "Lucent Technologies discloses the use of the ORT4622 half bridge (page 1, 4th paragraph) including field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and containing 'a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used), see page 1, 4th paragraph, for providing design flexibility, functionality, and performance." (See

Examiner's Answer, page 6 and 7). The Examiner alleged that the "ORT4622 half bridge is clearly "scalable" depending on the bandwidth needed and the fact that the ORT4622 half bridge contains a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used clearly indicates that less then 4 channels can be sued when less bandwidth is needed" (See Examiner's Answer, page 7).

As discussed above, Lucent Technologies fails to disclose or suggest the application scalability to connection of **TWO** half bridge circuits, i.e., fails to disclose or suggest a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26.

Moreover, as discussed above the Examiner alleges that "the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that the Applicants employ." (Examiner's Answer, page 7). The reason Lucent Technologies' ORT4622 is the same ORT4622 that Applicants employ is that the Examiner simply found a reference that **reiterates** what Applicants disclose in their specification. The Applicants are unsure of what purpose finding a prior art reference to reiterate what Applicants disclose in their specification served. Lucent Technologies STILL fails to disclose or suggest connection of **TWO** half bridge circuits for any reason, much less disclose or suggest a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26.

Moreover, as discussed above "Teachings of references can be combined only if there is some suggestion or incentive to do so." In re Fine, 5 USPQ2d 1596,1600 (Fed. Cir. 1988) (quoting ACS Hosp. Sys. v. Montefiore Hosp., 221 USPQ 929, 933 (Fed. Cir. 1984)) (emphasis in original). Nothing within Lange nor Lucent Technologies suggests modifying Lange to replace Lange's disclosed primary bridge and secondary bridge with two ORT4622s.

Thus, any modification of Lange without some suggested need to simply arrive at the claimed features is based on improper hindsight.

Official Notice is relied on to disclose two PCI buses having substantially same frequencies. Thus, Lange even in view of two PCI buses having substantially same frequencies STILL fails to disclose or suggest scalable signal lines between **TWO** half bridge circuits, i.e., fails to disclose or suggest a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26.

Accordingly, for at least all the above reasons, claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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